IN THE CLAIMS

1) Please amend Claims 1 and 12 as follows:

1. (Amended) A power monitor circuit [capable of notifying] operable to notify processing circuits operating from a first power supply having a VDD output voltage when a second power supply having a VDDIO output voltage is powered up, wherein VDDIO is greater than VDD, said power monitor circuit comprising:

a voltage divider circuit coupled between said second power supply and ground and having an output node that rises to a high voltage when said second power supply is powered up; and

an odd number of serially connected inverters operating from said first power supply, wherein an input of a first of said serially connected inverters is connected to said voltage divider circuit output node and an output of a last of said serially connected inverters produces a status signal that is low when said voltage divider circuit output node is high and is high when said voltage divider circuit output node is low, and wherein said status signal is an input signal to said voltage divider circuit operable to minimize DC current consumption in said voltage divider circuit when said second power supply is powered up while maintaining a value of said status signal.

12. (Amended) An integrated circuit comprising:

core processing circuitry operating from a first power supply having a VDD output voltage;

output stage circuitry operating from a second power supply having a VDDIO output voltage, wherein VDDIO is greater than VDD; and

a power monitor circuit [capable of notifying] operable to notify said core processing circuitry when said second power supply having said VDDIO output voltage is powered up, said power monitor circuit comprising:

a voltage divider circuit coupled between said second power supply and ground and having an output node that rises to a high voltage when said second power supply is powered up; and

an odd number of serially connected inverters operating from said first power supply, wherein an input of a first of said serially connected inverters is connected to said voltage divider circuit output node and an output of a last of said serially connected inverters produces a status signal that is low when said voltage divider circuit output node is high and is high when said voltage divider circuit output node is low, and wherein said status signal is an input signal to said voltage divider circuit operable to minimize DC current consumption in said voltage divider circuit when said second power supply is powered up while maintaining a value of said status signal.